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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/707,844	11/08/2000	Hidetoshi Ishida	0819-448	9493

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EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	**PAPER NUMBER**
2891	

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11/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/707,844	ISHIDA ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 6/14/07 have been fully considered but they are not persuasive. There are seven (7) arguments presented in response to the non-final rejection mailed on 3/15/07.

The first argument is that Inoue fails to teach a distance between two adjacent ones of the plurality of through holes is smaller than a thickness of the semiconductor substrate so as to reduce power leaking between two adjacent ones of the plurality of semiconductor elements. It is noted that Inoue fails to teach the thickness of the substrate, consequently it can't be optimized.

Please note that the rejection notes that this relationship isn't disclosed in Inoue. The rejection states that "Inoue does not expressly disclose a distance between two adjacent ones of the plurality of through holes is smaller than a thickness of the semiconductor substrate. Inoue, however, discloses that the through holes have spacing substantially less than a wavelength of the operating frequency of the circuits in the layer which the through holes are located at (see col. 4, lines 1-5). Noting that the through holes are formed in and over the substrate, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the distance between the through holes smaller than the thickness of the substrate to further insulate the integrated circuits of the substrate from RF interfering." Further, Inoue teaches "The shielding means has a spacing density and height above the substrate adapted to block

electromagnetic radiation between the circuits" (3, 22+). With these two teaching in mind, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize this distance through routine experimentation (MPEP 2144.05).

The second argument is that Inoue teaches the through holes through the insulating layer and not the semiconductor substrate.

Please note that Inoue clearly teaches forming the through holes through the semiconductor substrate [Figure 1, reference # 23b & (5, 32+)].

The third argument is that Inoue's teaching that the through holes are spaced substantially less than the operating frequency (5, 1-5) teaches away from the claimed invention because the operating frequency is greater than the thickness of the substrate already since the insulating layer is thickness is set at 500 um.

While that may be true, and it isn't being conceded as such, it doesn't change the fact that the through holes are also formed within the semiconductor substrate and this relationship must also be considered within said semiconductor substrate. The relationship between the insulating layer is irrelevant when considering the semiconductor substrate.

The fourth argument is that both Inoue and Nakamura fail to teach the through holes for shielding and for electrodes are formed simultaneously, as in claim 15.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., through holes for shielding and for electrodes are formed simultaneously) are not recited in the rejected claim(s). Although the claims are interpreted in light of the

specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The fifth argument is that Nakamura fails to teach the distance between two adjacent through holes is small so as to improve isolation between two adjacent semiconductor elements.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Please note that Nakamura isn't relied upon to teach this relationship. Inoue is relied upon to teach it.

The sixth argument is that neither Inoue nor Nakamura teach the combination of through holes for shielding and through holes for electrodes.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The rejection states that the combination of Inoue and Nakamura teach this limitation, not either one individually. The rejection states "it would have been obvious to one of ordinary skill in the art at the time of the invention to make connection to the semiconductor devices of the Inoue in the fashion of the Nakamura reference (which would lead to their connection to the backside ground wiring 52), commonly known as

flip chip structure, in order to make contacts to the semiconductor components of the Inoue, and provide a ground voltage reference for those devices. Flip chip configurations and their advantages, such as occupying less space and making secure contacts are well known in the art."

The seventh, and final, argument regarding claims 20 and 21 is that the references fail to teach connecting elements of the RF device to a wiring layer. Please note that Inoue does indeed teach a wiring layer [32] (5, 26+), which would/could attach to a PCB. The PCB would be obvious to a skilled artisan because it is the conventional next level of integration. Meaning, in order to use the RF device, it must be attached to other electrical substrates, such as a PCB. The use of conventional materials to perform their known functions is obvious (MPEP 2144.07).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 11-14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US Patent 5,151,770).

Regarding claims 11, 14, 17 and 18, Inoue discloses in figure 1, a semiconductor device comprising:

a plurality of semiconductor elements, 24 and 26, formed on a semiconductor substrate 21, 27 composed of a semiconductor material; and

a plurality of through holes, which are provided between two adjacent ones of the plurality of semiconductor elements and pass from a surface through the backside of the semiconductor substrate, which is GaAs (see figure 5, and col. 9, lines 29-32).

Inoue does not expressly disclose a distance between two adjacent ones of the plurality of through holes is smaller than a thickness of the semiconductor substrate. Inoue, however, discloses that the through holes have spacing substantially less than a wavelength of the operating frequency of the circuits in the layer which the through holes are located at (see col. 4, lines 1-5). Noting that the through holes are formed in and over the substrate, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the distance between the through holes smaller than the thickness of the substrate to further insulate the integrated circuits of the substrate from RF interfering.

Regarding claim 12, the through holes are covered with a conductive material (see col. 8, lines 1-5).

Regarding claim 13, the conductive material is electrically connected to a ground wiring layer 52 (figs. 4 and 5) provided on the surface of the backside of the substrate (see col. 8, lines 1-5).

Claims 15, 16 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue as applied to claims 11-14 above, and further in view of Nakamura et al., hereinafter Nakamura (US Patent 6,229,209).

Regarding claims 15 and 16, Inoue discloses the limitations in the claims, as discussed above, except for a second group of through holes which are provided in electrodes of the plurality of semiconductor elements, pass from a surface through the backside of the substrate, and whose faces are covered with conductive material.

Nakamura discloses in figure 1, a second group of through holes 23 which are provided in electrodes of the semiconductor element 3, pass from a surface through the backside of the substrate 20, and whose faces are covered with conductive material 24 (see col. 6, lines 4-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make connection to the semiconductor devices of the Inoue in the fashion of the Nakamura reference (which would lead to their connection to the backside ground wiring 52), commonly known as flip chip structure, in order to make contacts to the semiconductor components of the Inoue, and provide a ground voltage reference for those devices. Flip chip configurations and their advantages, such as occupying less space and making secure contacts are well known in the art.

Regarding claims 19-21, any two of the through holes 23 and the corresponding wirings 22 can be thought of as a group of through holes with one or more corresponding wirings. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to interconnect the ground layer of the Inoue reference to some wiring layers of the Nakamura reference in order to establish a ground voltage reference for the structure as a whole.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David A. Zarneke/
Primary Examiner
November 16, 2007